CLAIM AMENDMENTS

The following is a complete listing of the pending claims:

1. (currently amended) A differential charge pump, comprising:

a current switch responsive to a pulse width difference between a differential up voltage and a differential down voltage to source and sink a current in a complementary fashion from a pair of differential output nodes, wherein the differential output nodes are voltage isolated from the current switch;

a first transconductance amplifier configured to convert a voltage at a first one of the differential output nodes into a first current; and

a second transconductance amplifier configured to convert a voltage a second one of the differential output nodes into a second current that is complementary to the first current.

2. (original) The charge pump of claim 1, further comprising:

a resistive load coupled between a first node and a second node, wherein the first transconductance amplifier is configured to couple the first current to the first node and the second transconductance amplifier is configured to couple the second current to the second node.

3. (original) The charge pump of claim 2, further comprising a common-mode feedback circuit configured to maintain a common-mode voltage on the resistive load equal to a common-mode reference voltage.

4. (original) The charge pump of claim 1, wherein the first and second transconductance amplifiers are operational transconductance amplifiers.

5. (currently amended) The charge pump of claim 2 4, wherein the current switch comprises:

a first differential pair of transistors biased by a first current source to conduct the current, the transistors in the first differential pair being responsive to the differential up voltage such that when the differential up voltage is pulsed the current is conducted by a first transistor in the first differential pair and when the differential up voltage is not pulsed the current is conducted by a remaining second transistor in the first differential pair; and

a second differential pair of transistors biased by a second current source to conduct the current such when the differential down voltage is pulsed the current is conducted by a first transistor in the second differential pair and when the differential up voltage is not pulsed the current is conducted by a remaining second transistor in the second differential pair.

6. (currently amended) The charge pump of claim 5, wherein the common-mode feedback circuit includes:

a first current source configured to source twice the current to a first node; and

a second current source configured to source twice the current to a second node, wherein the first transistor in the first differential pair and the

second transistor in the second differential pair couples to the first node through a first pair of resistors ~~resistive loads~~, and wherein the second transistor in the first differential pair and the first transistor in the second differential couples to the second node through a second pair of resistors, whereby the first and second pairs of resistors perform the voltage isolation of the current switch from the differential output nodes ~~resistive loads~~.

7. (original) The charge pump of claim 6, wherein the first and second transistors in the first and second differential pairs are NMOS transistors.

8. (currently amended) A differential phase-locked loop (PLL), comprising:

a phase detector configured to compare a feedback signal to a reference signal to produce a differential up voltage and a differential down voltage; and

a charge pump including a current switch responsive to a pulse width difference between the differential up voltage and the differential down voltage to source and sink a current in a complementary fashion from a pair of differential output nodes, wherein the differential output nodes are voltage isolated from the current switch, the charge pump including a common-mode feedback circuit configured so that the differential output nodes charge and discharge with respect to a common mode voltage, and wherein the common-mode feedback circuit is isolated from the differential output nodes through transconductance amplifiers.

9. (original) The differential PLL of claim 8, further comprising:

a loop filter configured to filter voltages at the differential output nodes to provide a filtered differential output voltage;

a voltage-controlled oscillator configured to provide an output signal having a frequency dependent upon the filtered differential output voltage; and

a loop divider configured to divide the output signal to provide the feedback signal.

10. (cancelled)

11. (original) The differential PLL of claim 10, wherein the current switch comprises:

a first differential pair of transistors biased by a first current source to conduct the current, the transistors in the first differential pair being responsive to the differential up voltage such that when the differential up voltage is pulsed the current is conducted by a first transistor in the first differential pair and when the differential up voltage is not pulsed the current is conducted by a remaining second transistor in the first differential pair; and

a second differential pair of transistors biased by a second current source to conduct the current such when the differential down voltage is pulsed the current is conducted by a first transistor in the second differential pair and when the differential up voltage is not pulsed the current is conducted by a remaining second transistor in the second differential pair.

12. (currently amended) The differential PLL of claim 11, wherein the common-mode feedback circuit includes:

a first current source configured to source twice the current to a first node; and

a second current source configured to source twice the current to a second node, wherein the first transistor in the first differential pair and the second transistor in the second differential pair couples to the first node through a first pair of resistors ~~resistive loads~~, and wherein the second transistor in the first differential pair and the first transistor in the second differential couples to the second node through a second pair of resistors, whereby the first and second pairs of resistors perform the voltage isolation of the current switch from the differential output nodes ~~resistive loads~~.

13. (original) The differential PLL of claim 12, wherein the transistors in the first and second differential pairs are NMOS transistors.

14. (currently amended) A method of operating a differential charge pump, comprising:

comparing the pulse widths of a differential up voltage and a differential down voltage using differential pairs of transistors;

generating a positive differential control voltage at a first differential output node and a negative differential control voltage at a second differential output

node responsive to the pulse width comparison, the nodes being voltage isolated from the differential pairs of transistors;

converting the positive differential control voltage into a first current using a first transconductance amplifier; and

converting the second differential control voltage into a second current using a second transconductance amplifier.

15. (original) The method of claim 14, further comprising:

converting the first and second currents into a common-mode voltage; and

altering the charge of the first and second differential output nodes to maintain the common-mode voltage equal to a reference common-mode voltage.

16. (original) The method of claim 15, further comprising:

filtering the positive and negative differential control voltages to provide a filtered differential voltage; and

driving a voltage-controlled oscillator with the filtered differential voltage to produce an output signal.

17. (original) The method of claim 16, further comprising:

dividing the output signal into a feedback signal.

18. (original) The method of claim 17, further comprising:

comparing the feedback signal to a reference signal; and

generating the differential up and down voltages in response to the comparison of the feedback signal to the reference signal.

19. (original) The method of claim 18, wherein the reference signal is a reference clock signal and wherein the output signal is an output clock signal.